FIG. 1 PRIOR ART

BLOCK DIAGRAM SHOWING CONFIGURATION OF CONVENTIONAL MULTIPLICATION PLL CIRCUIT

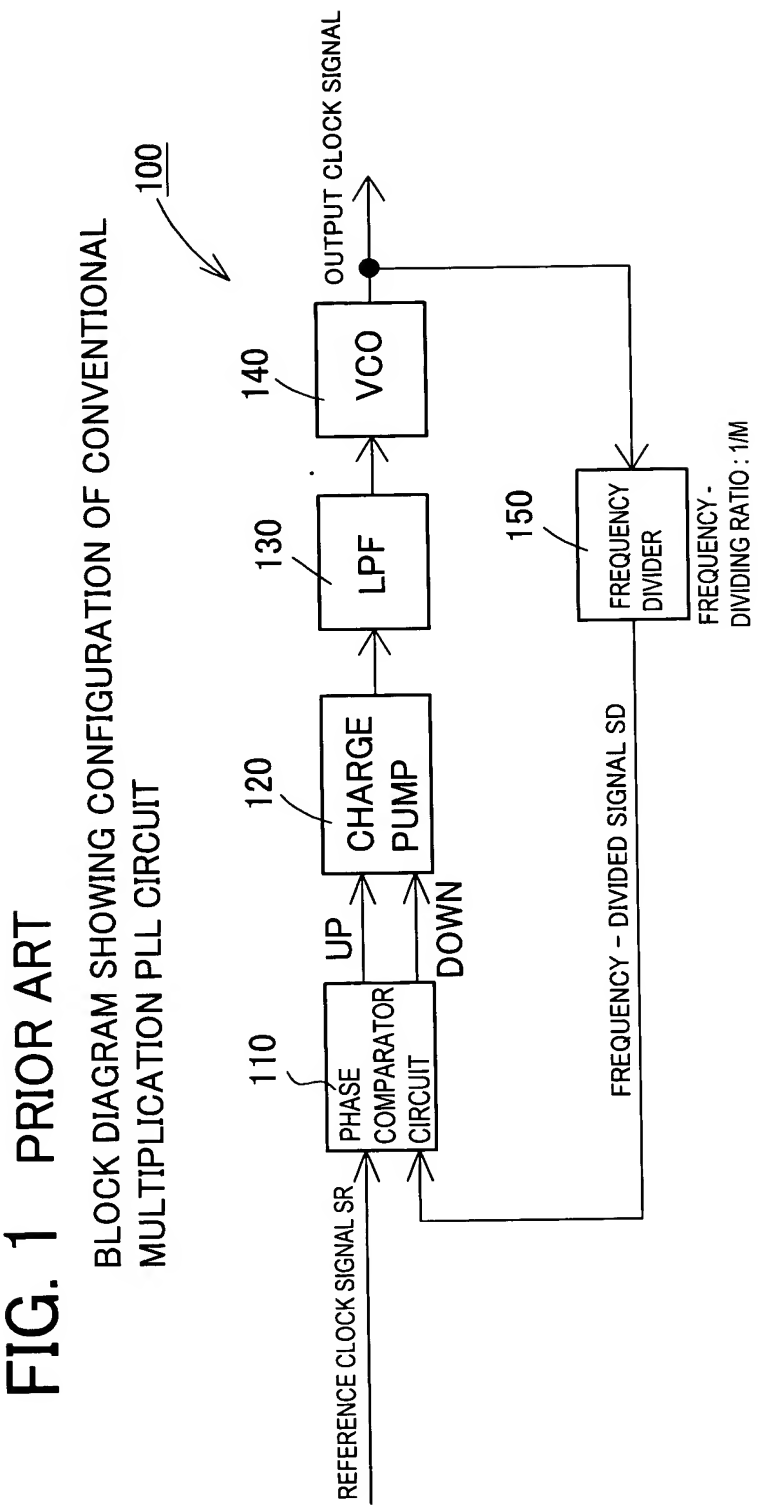

FIG. 2

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 1

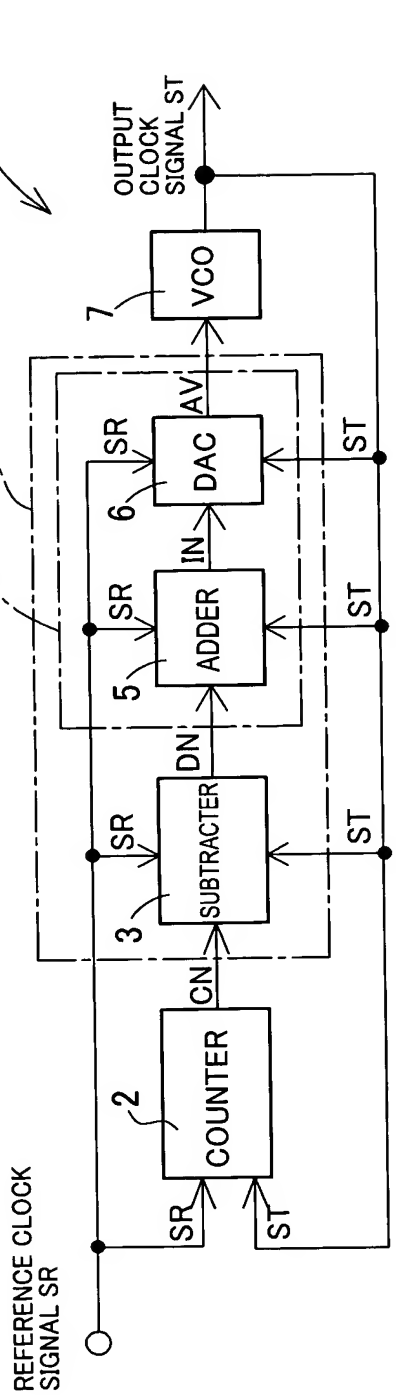

FIG. 3

TIME CHART SHOWING ACTION OF RESPECTIVE COMPONENTS OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 1

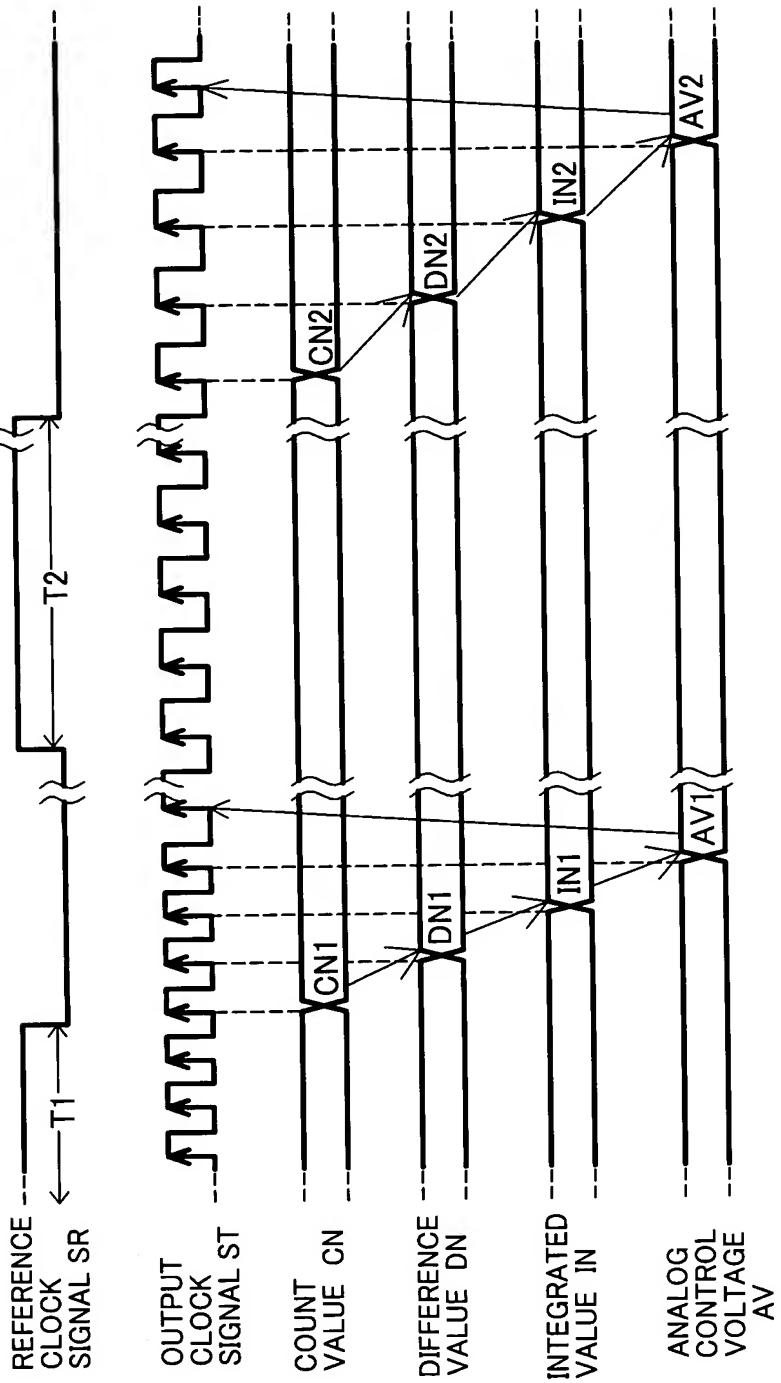

FIG. 4

TIME CHART SHOWING ACTION OF RESPECTIVE COMPONENTS OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 1

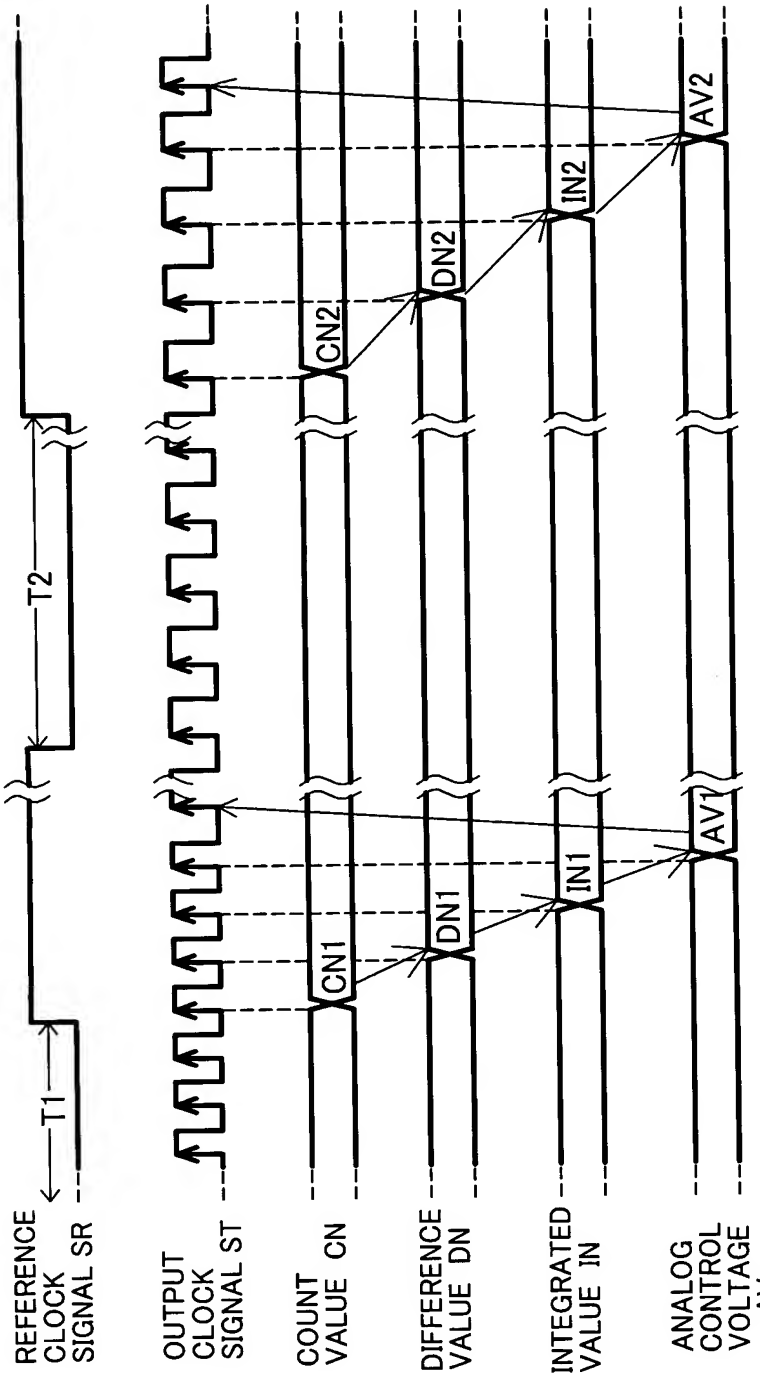

FIG. 5

TIME CHART SHOWING ACTION OF RESPECTIVE COMPONENTS OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 2

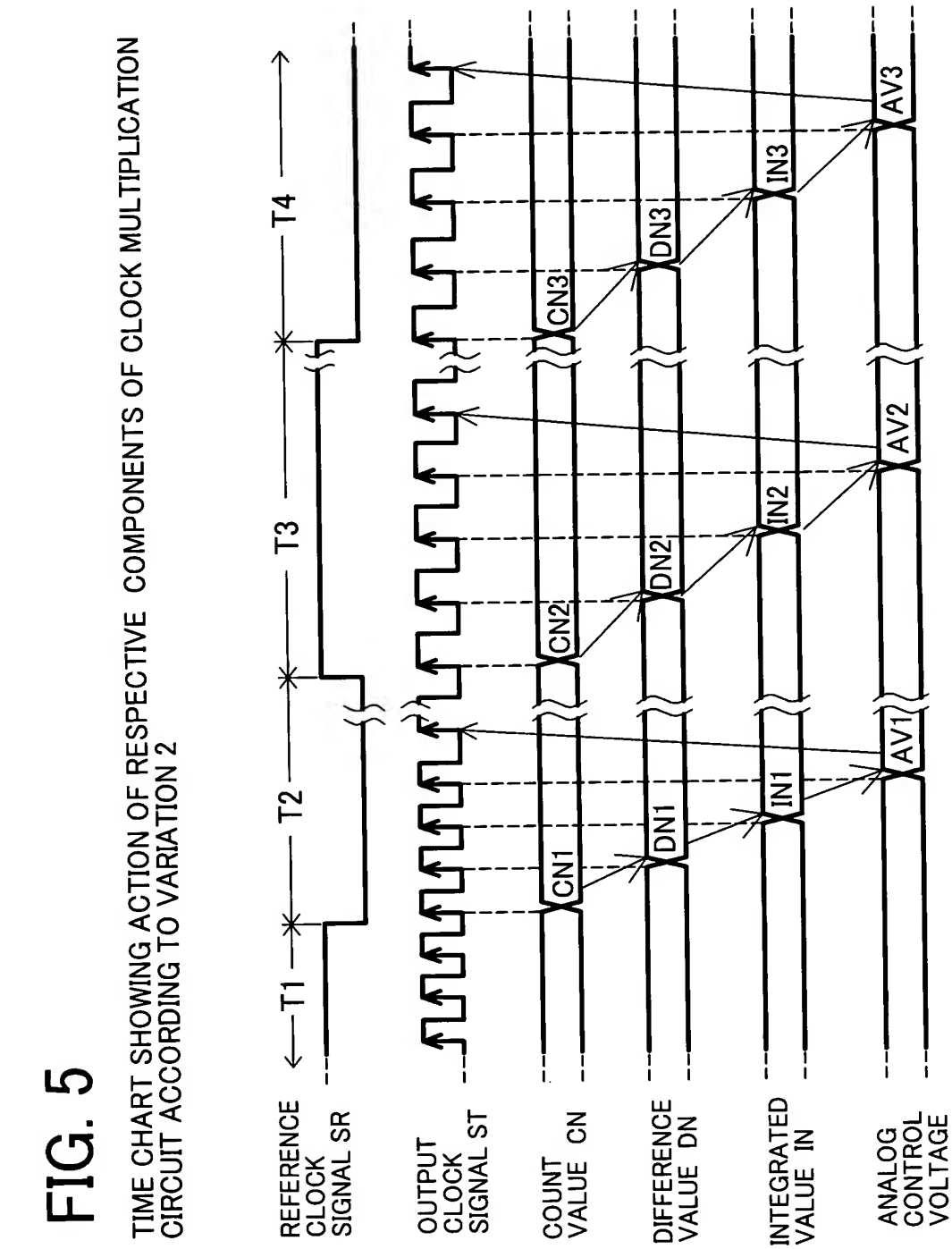

FIG. 6

SCHEMATIC DIAGRAM ILLUSTRATING FLUCTUATION OF OUTPUT CLOCK SIGNAL AT TIME OF COUNTING RISING EDGES OF OUTPUT CLOCK SIGNAL FOR CONTROL

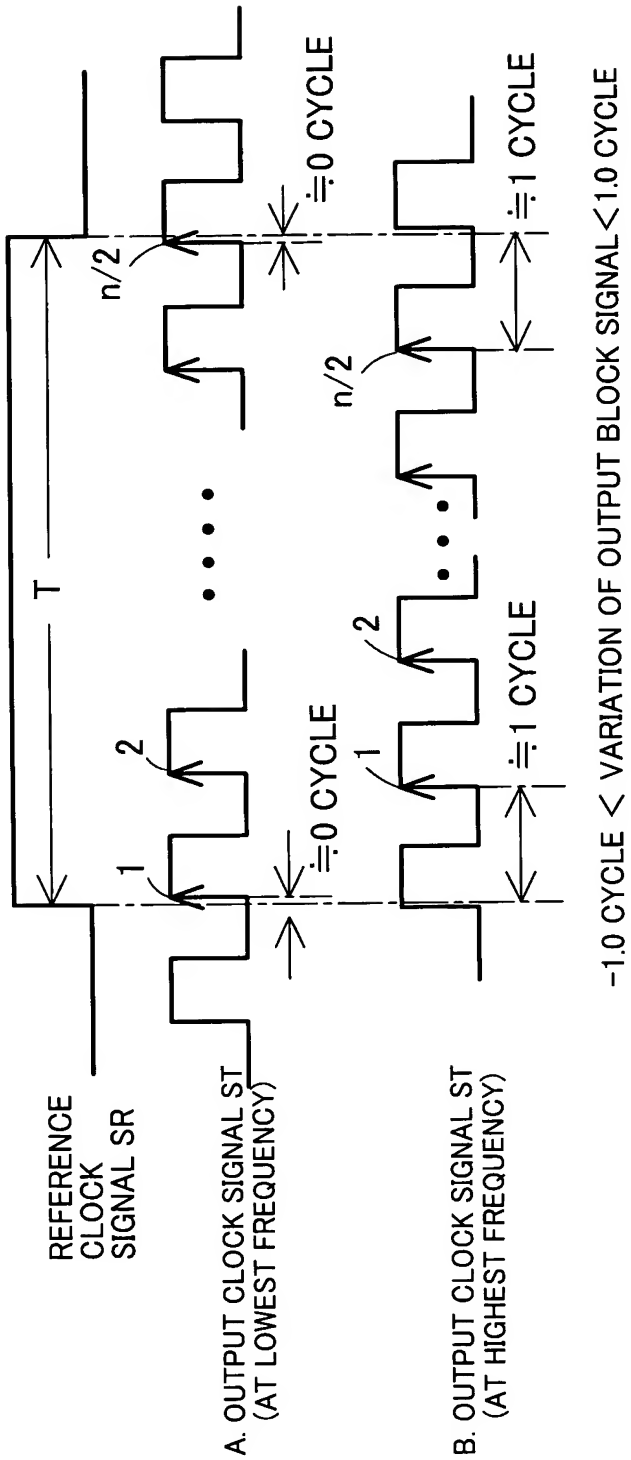

FIG. 7

SCHEMATIC DIAGRAM ILLUSTRATING FLUCTUATION OF OUTPUT CLOCK SIGNAL AT TIME OF COUNTING BOTH RISING EDGES AND FALLING EDGES OF OUTPUT CLOCK SIGNAL FOR CONTROL ACCORDING TO VARIATION 3

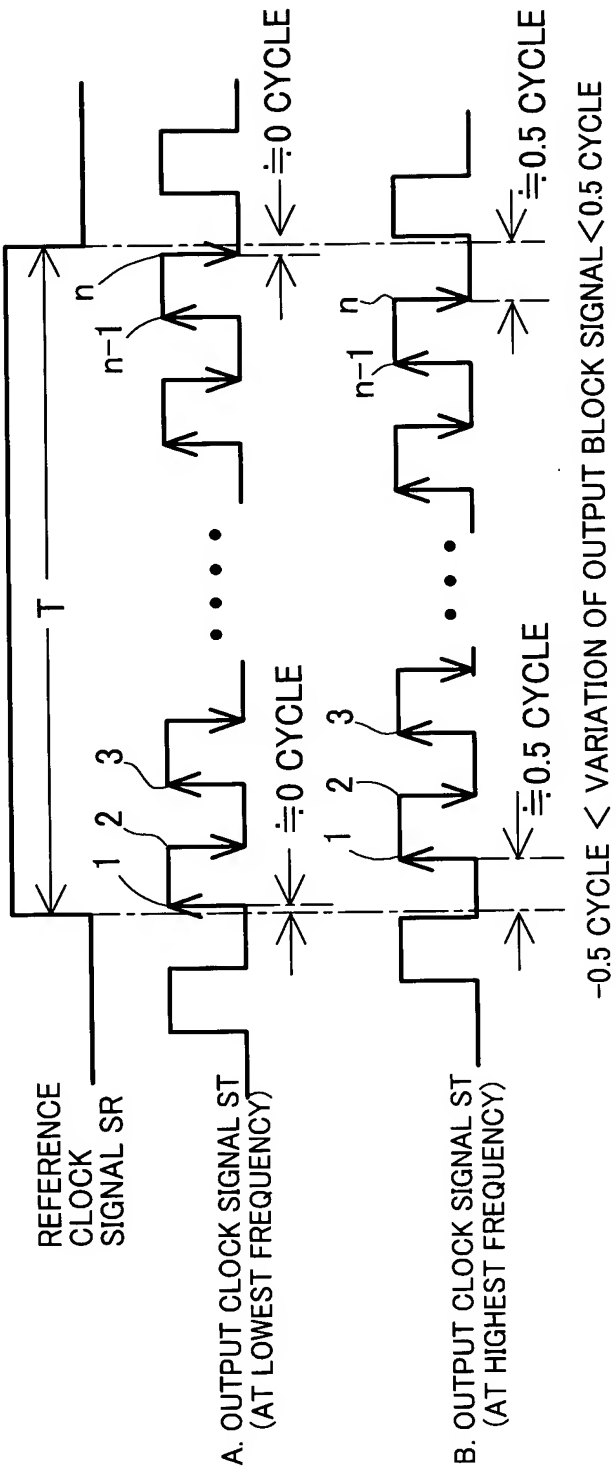

FIG. 8

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 2

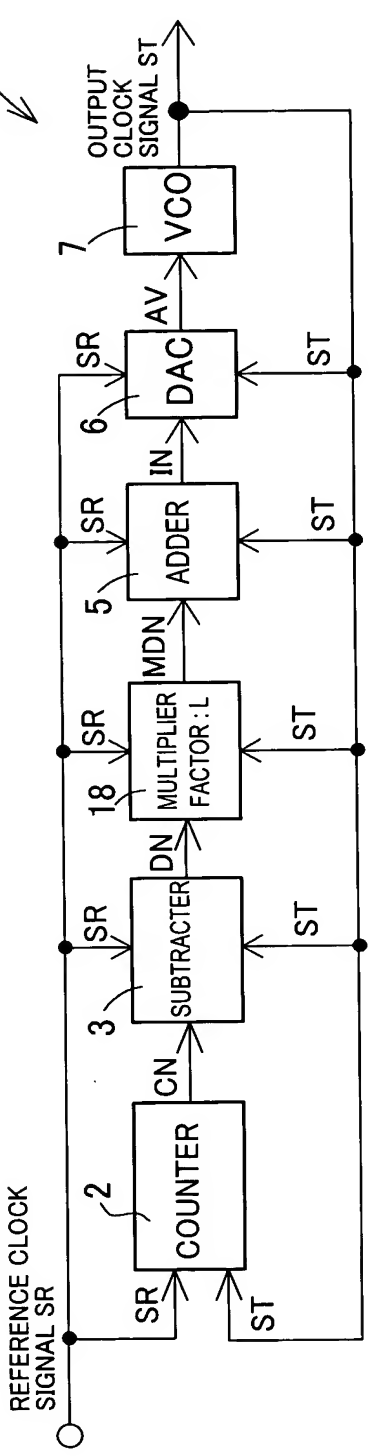

FIG. 9

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 4

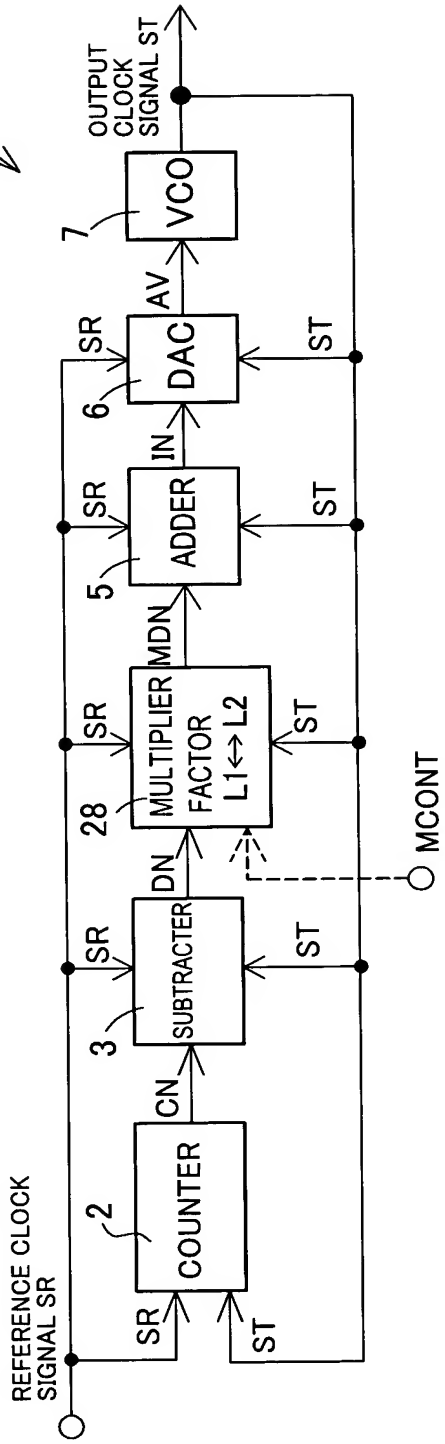

FIG. 10

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 5

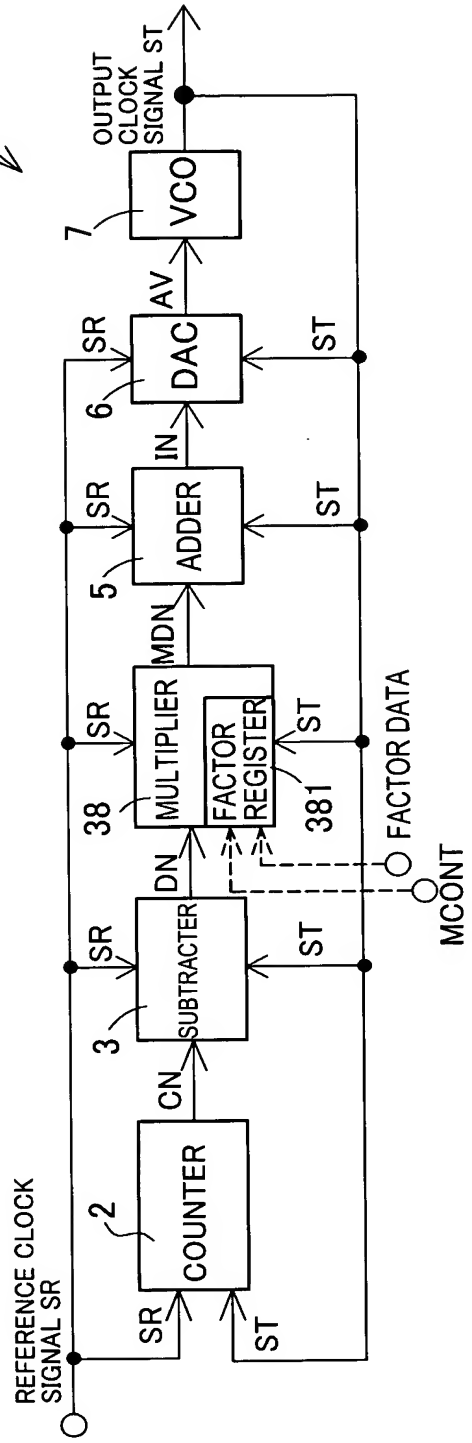

FIG. 11

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 3

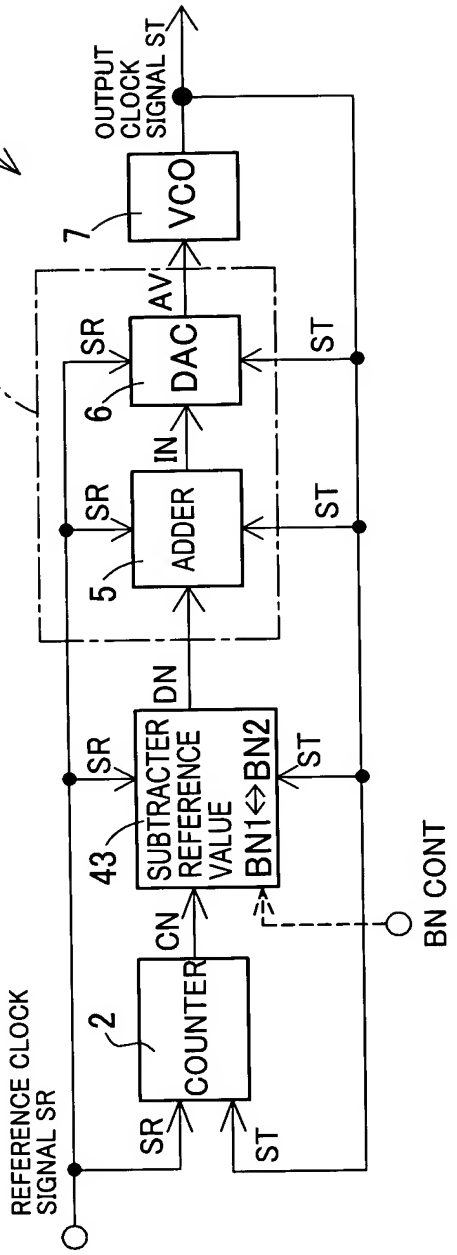

FIG. 12

SCHEMATIC DIAGRAM SHOWING CONFIGURATION OF SUBTRACTER OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 3

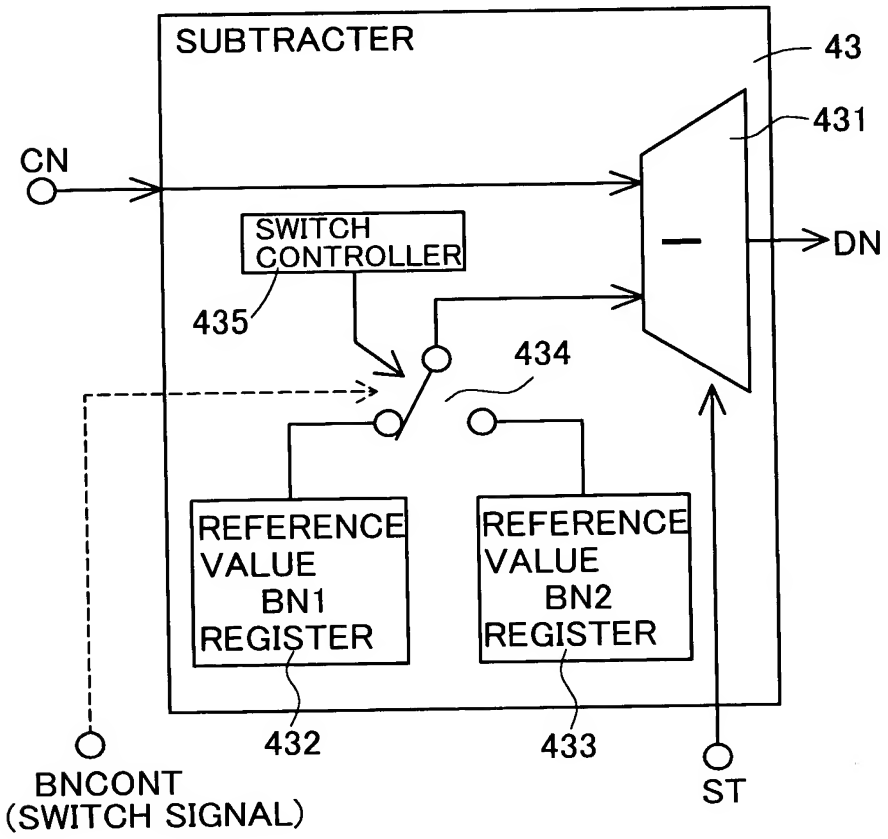

FIG. 13

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 6

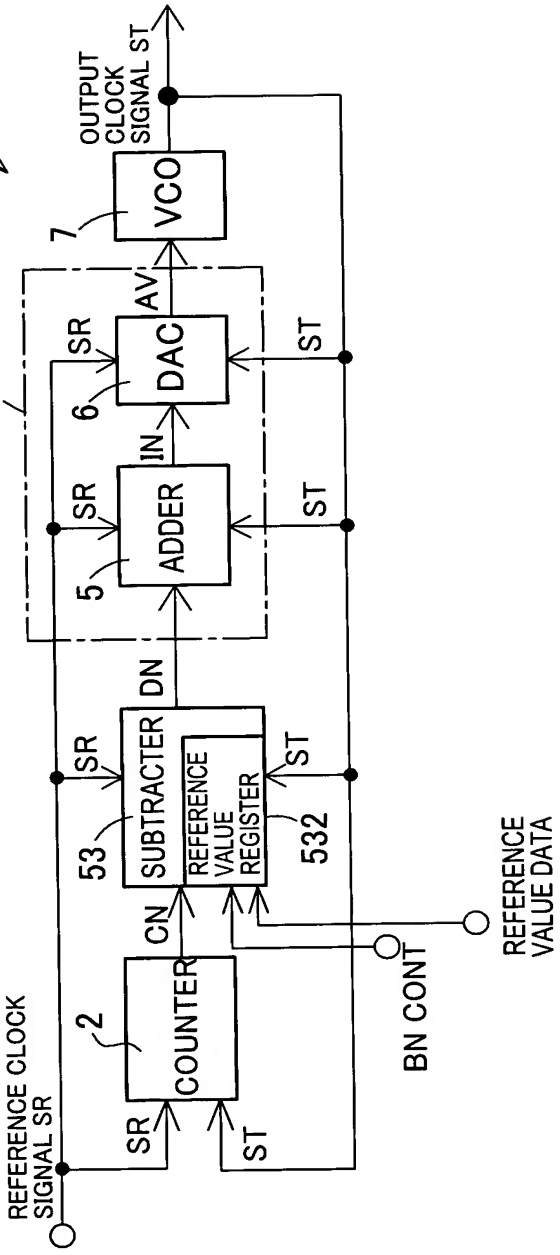

FIG. 14

SCHEMATIC DIAGRAM SHOWING CONFIGURATION OF SUBTRACTER OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 6

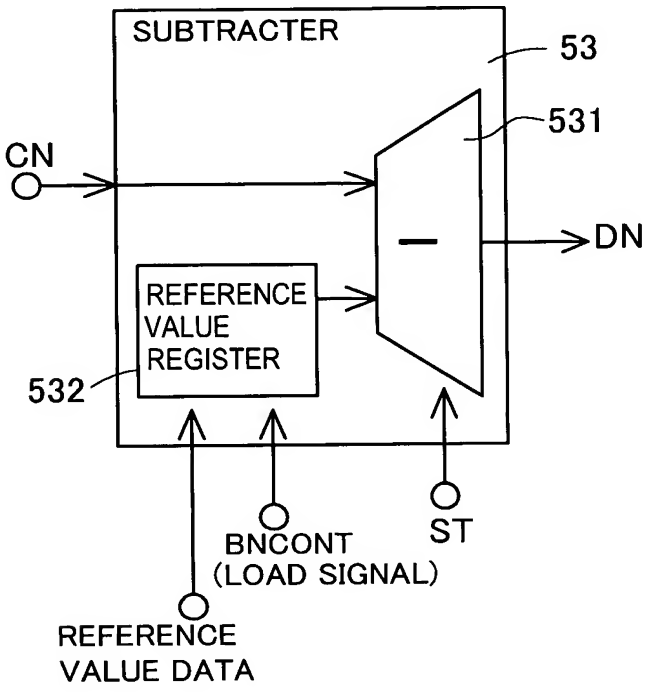

FIG. 15

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 4

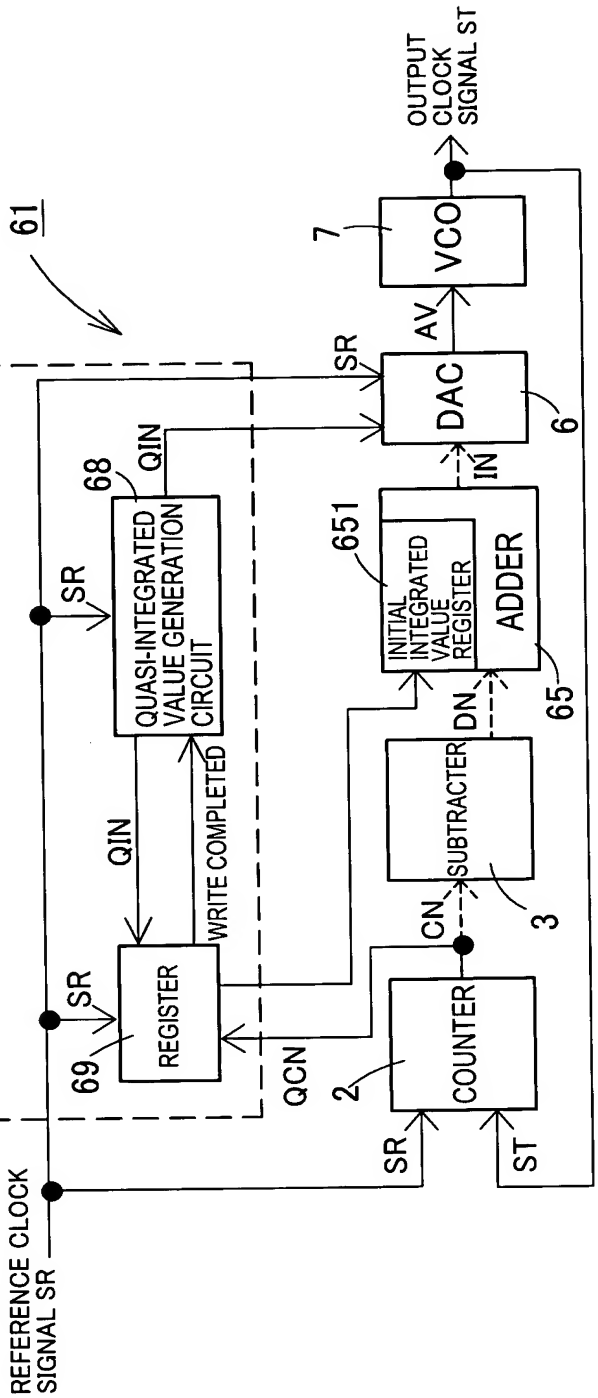

FIG. 16

FLOW CHART OF OPERATION SHOWING STEPS OF OBTAINING INITIAL INTEGRATED VALUE IN CASE OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 4

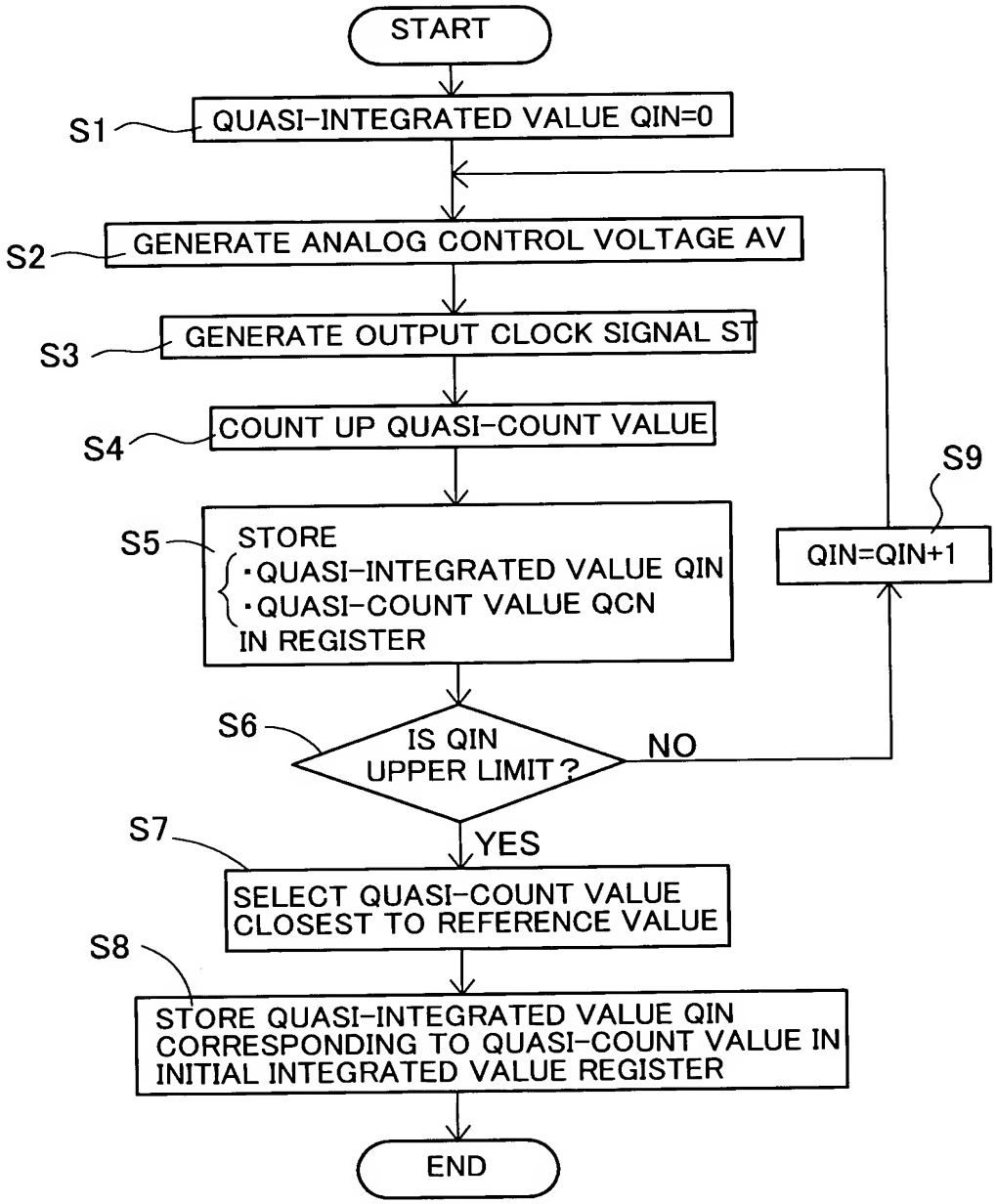

FIG. 17

EXAMPLE OF STORING QUASI-INTEGRATED VALUE TOGETHER WITH QUASI-COUNT VALUE IN A REGISTER OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 4

ADDRESS	QUASI-INTEGRATED VALUE QIN	QUASI-COUNT VALUE QCN
00h	00000000	00000110
01h	00000001	00000111
02h	00000002	00001001
03h	00000003	00001010
⋮	⋮	⋮
FEh	11111110	01101100
FFh	11111111	01101110

FIG. 18

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 7

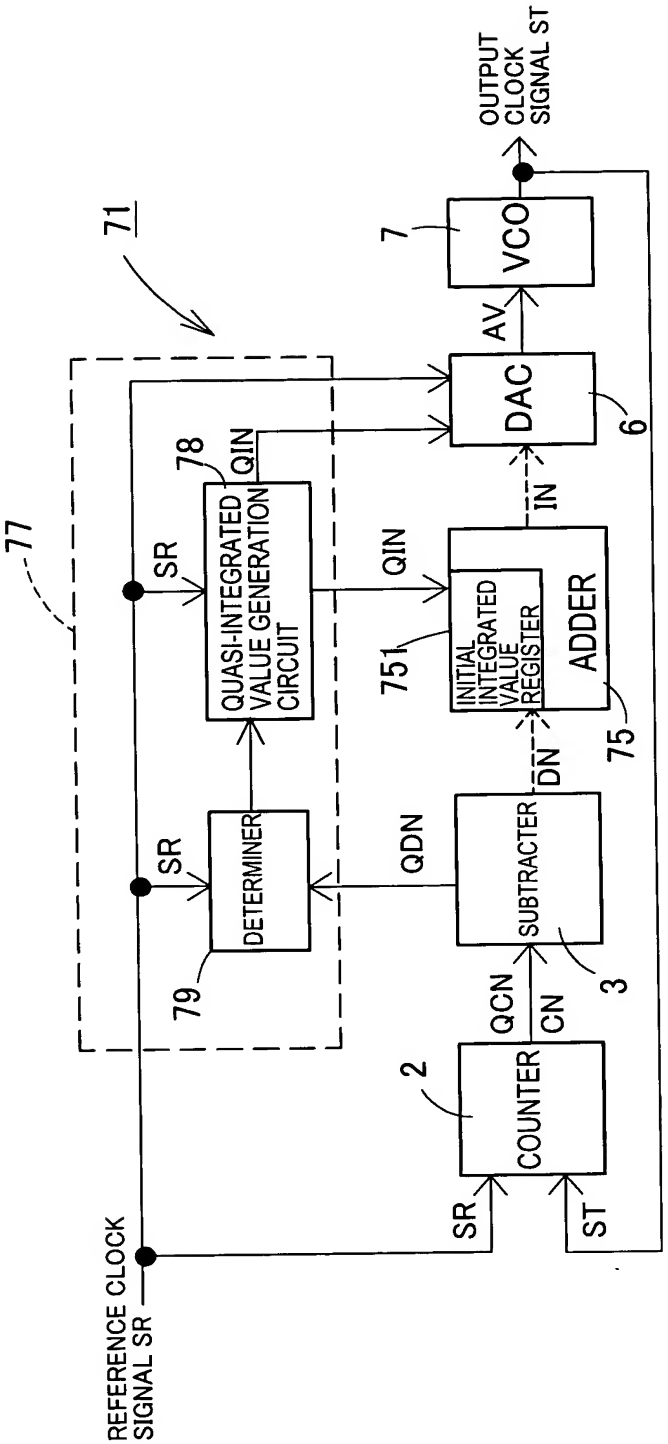

FIG. 19

FLOW CHART OF OPERATION SHOWING STEPS OF OBTAINING INITIAL INTEGRATED VALUE IN CASE OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 7

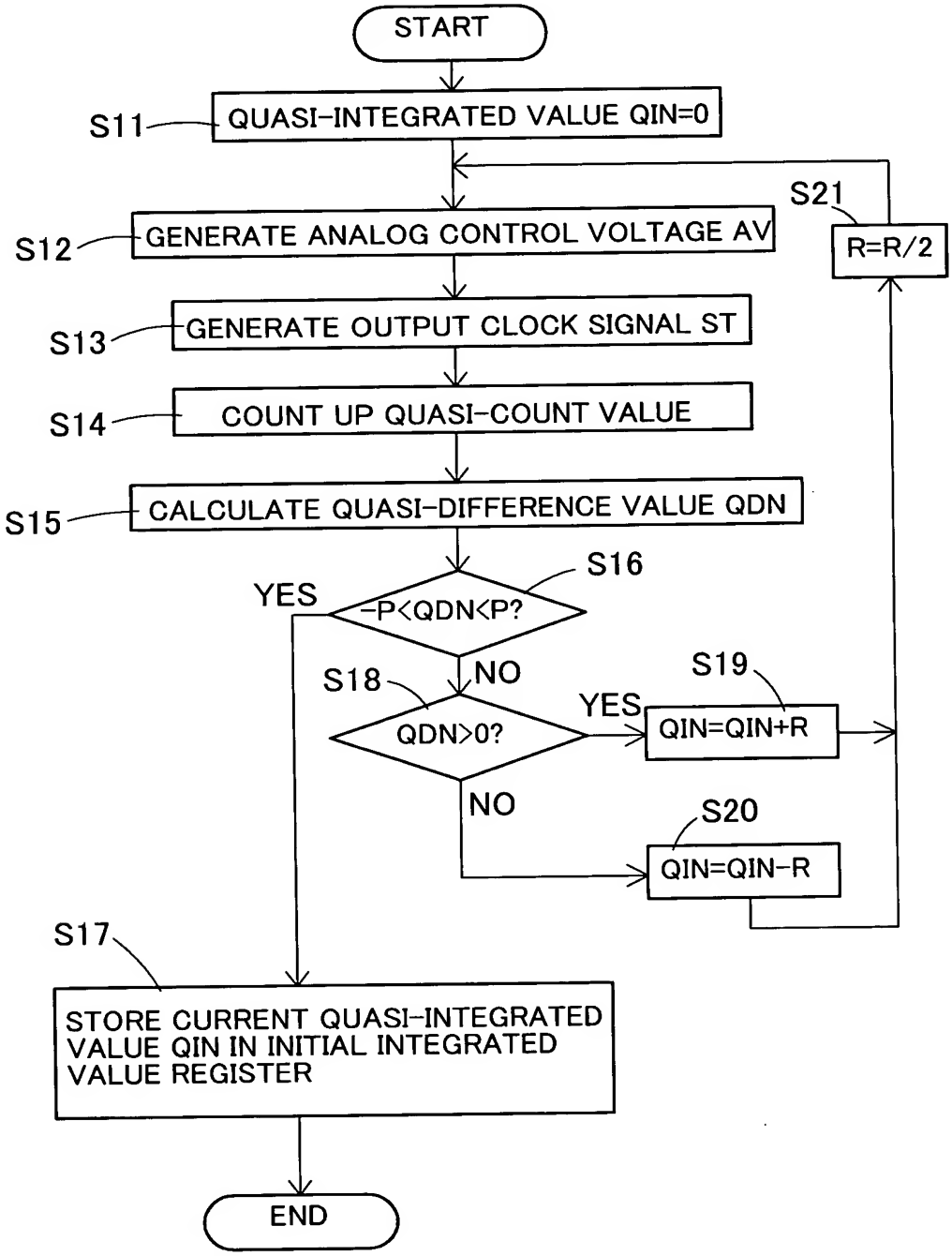

FIG. 20

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 8

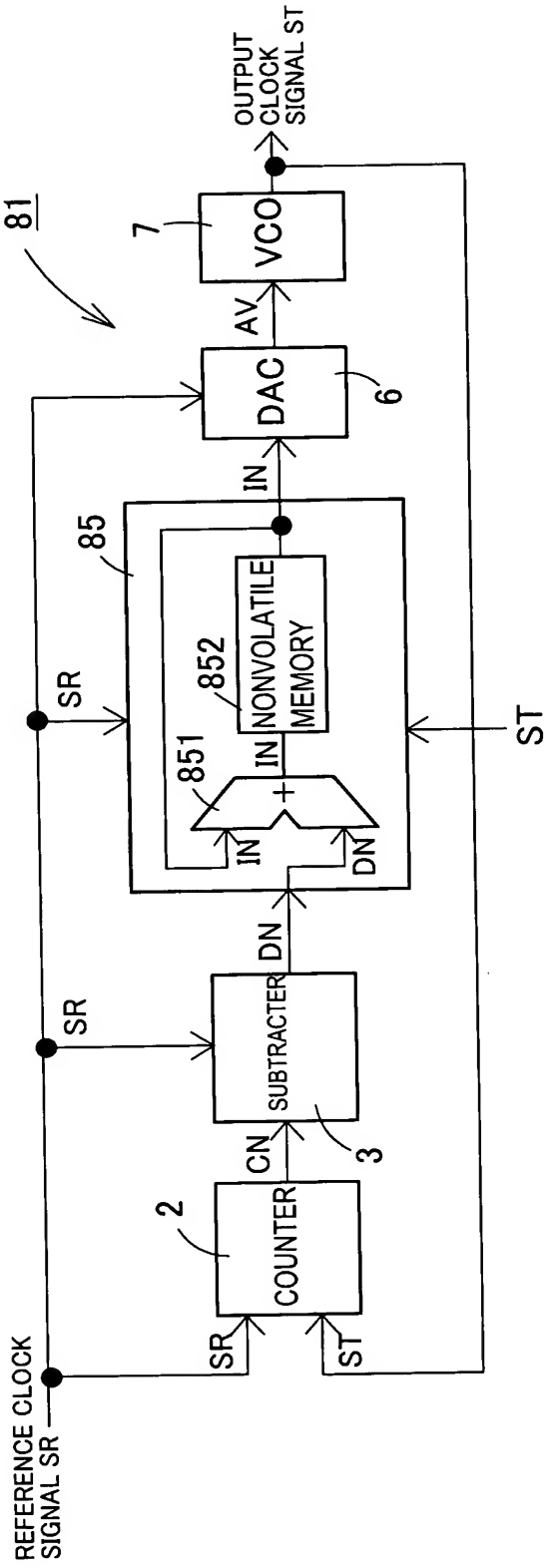

FIG. 21

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 9

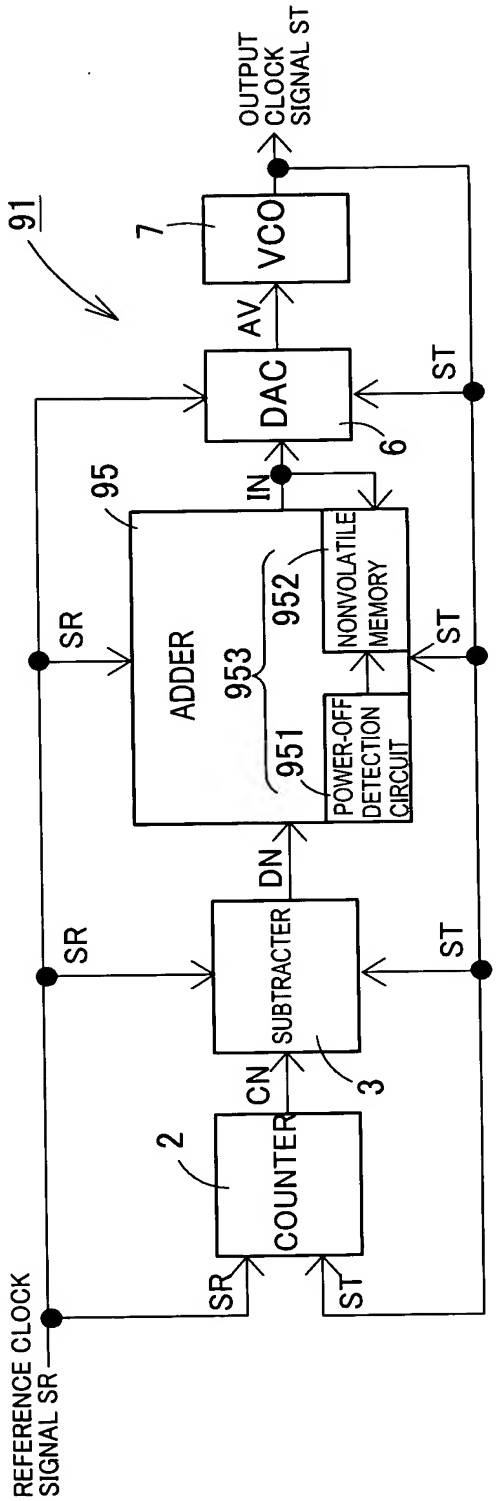

FIG. 22

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO VARIATION 10

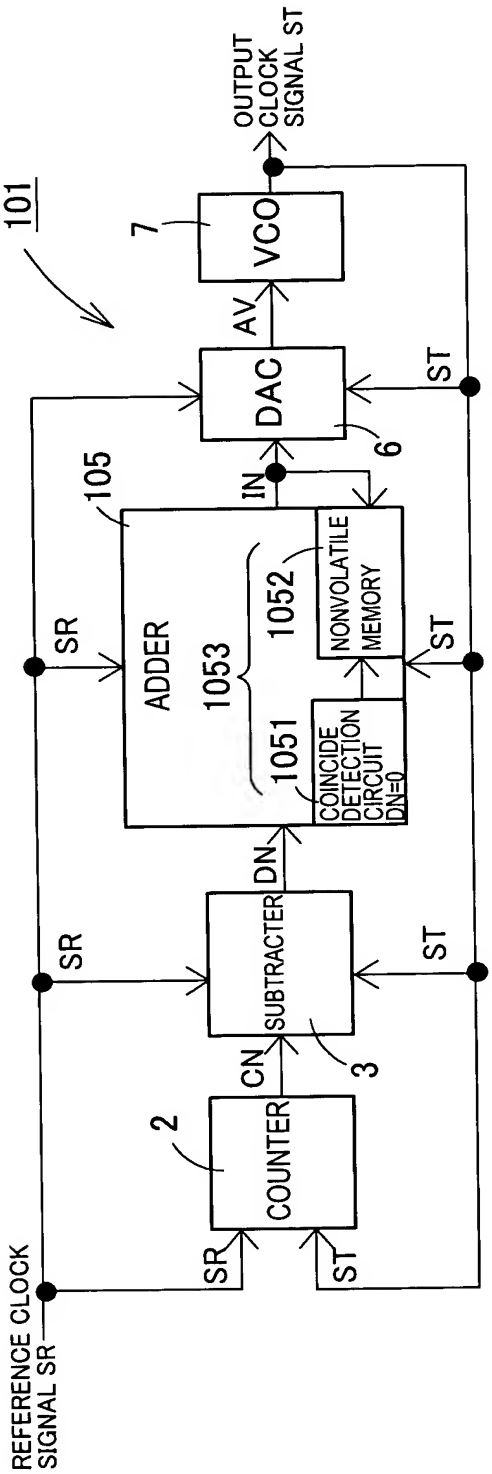

FIG. 23

BLOCK DIAGRAM SHOWING CONFIGURATION OF CLOCK MULTIPLICATION CIRCUIT ACCORDING TO EMBODIMENT 5